RECEIVED
CENTRAL FAX CENTER
NOV 2 1 2006

REMARKS

Applicant appreciates the withdrawal of the rejections of the claims over Liaw.

Applicant hereby adds new claims 105-108. Accordingly, claims 21-30 and 61-108 are pending in the present application.

Claims 21-30 and 61-82 stand rejected under 35 USC 102(b) for anticipation by Liou et al. ('268).

Applicant respectfully requests reconsideration of the rejections.

Referring to the anticipation rejections, Applicant notes the requirements of MPEP §2131 (8th ed., rev. 5), which states that TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM. The **identical invention** must be shown in as complete detail in the prior art as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). **The elements of the prior art must be arranged as required by the claim**. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Referring to independent claim 21, the semiconductor processing method recites *forming two series of field effect transistors and one series is isolated from adjacent devices by shallow trench isolation*. The Office on page 2 of the Action and without identification of any teachings in Liou states that Liou teaches forming two series of FETs over a substrate and one being isolated from adjacent devices by STI. Applicants have failed to uncover any teachings in Liou of the claimed forming two series of field effect transistors in combination with the claimed one series being isolated from adjacent devices by shallow trench isolation as claimed. Applicants respectfully submit that positively recited limitations are not disclosed by the prior art and claim 21 is

allowable for at least this reason.

The claims which depend from independent claim 21 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Referring to independent claim 26, the semiconductor processing method recites *forming two series of field effect transistors and at least one series is isolated from adjacent devices by shallow trench isolation*. The Office on page 3 of the Action identifies reference 28 of Fig. 2f of Liou in support of the rejection as allegedly teaching the STI limitations. It is clear from the teachings of col. 8, lines 60+ of Liou that reference 28 is a thermal oxide layer. Applicants have failed to uncover any teachings in Liou that reference 28 discloses shallow trench isolation. Applicants respectfully submit that positively recited limitations are not disclosed by the prior art and claim 26 is allowable for at least this reason.

The claims which depend from independent claim 26 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Applicants submit an Information Disclosure Statement herewith.

Applicants hereby add new claims 105-108 which are supported at least by the teachings in Figs. 2-4 and the respective associated teachings of the specification.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is

available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

11/21/06
Date

James D. Shaurette
Reg. No. 39,833
Reg. No. 39,833